

ADC12DX00RF Reference Board

REFERENCE DESIGN

SPECIAL NOTES

These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.

Since this product is in development, the user of this document is strongly advised to check for the latest revision.

National Semiconductor reserves the right to make changes to this product.

ALL parts labeled "NA" are NOT ASSEMBLED.


Print Instructions:

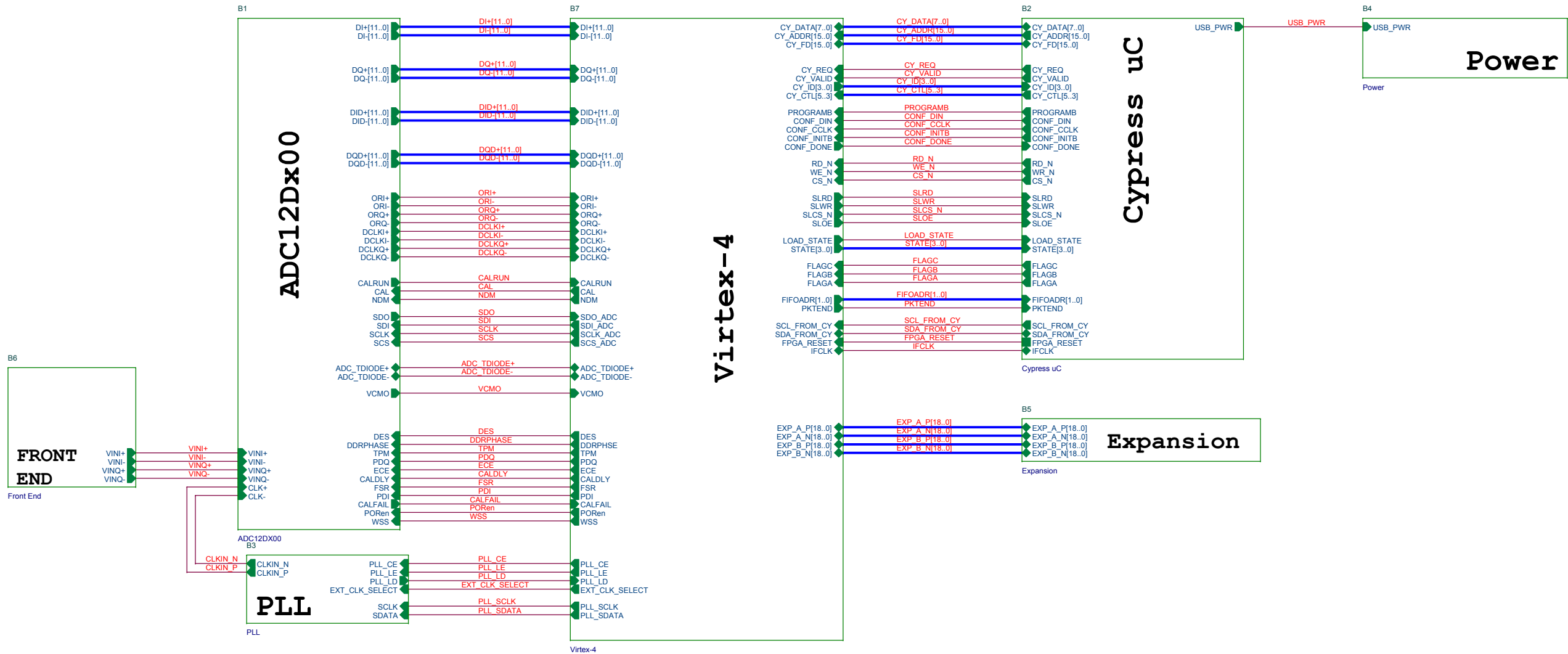
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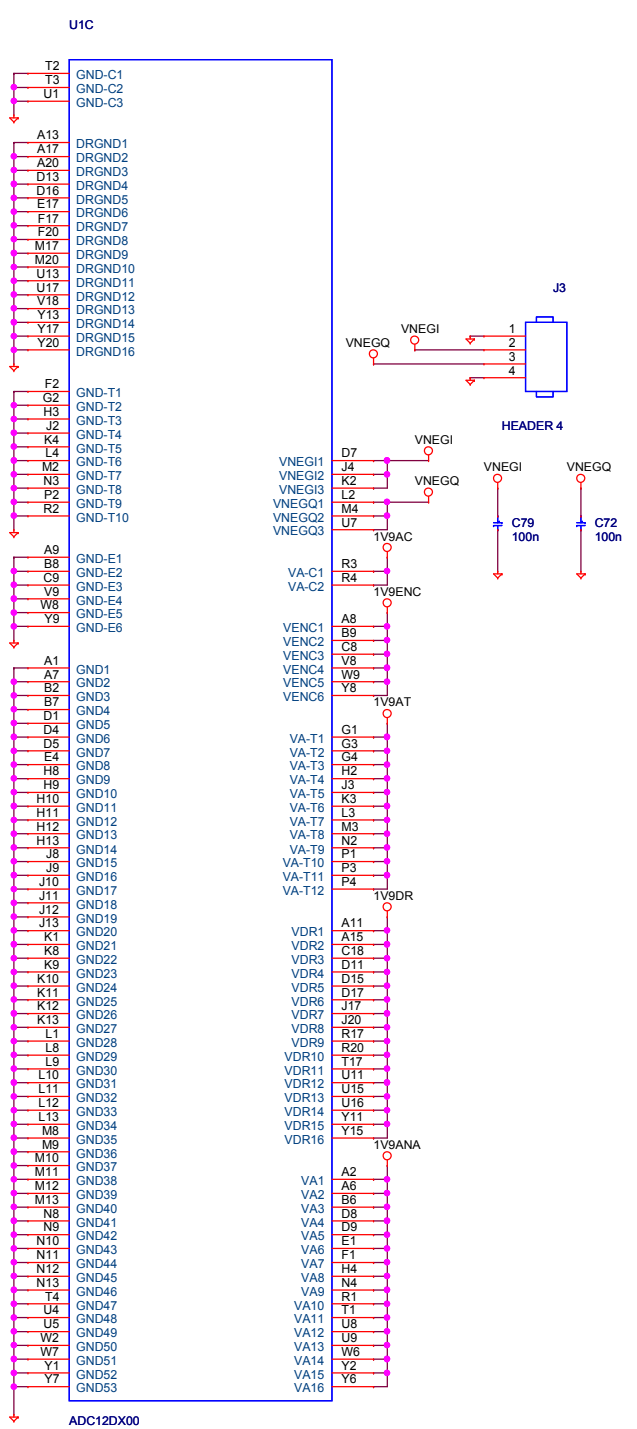
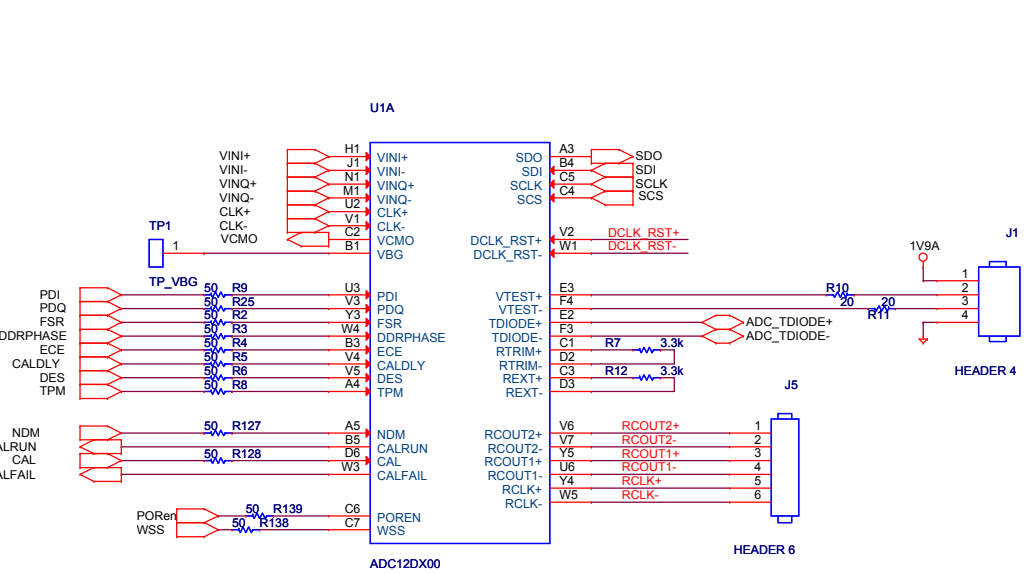
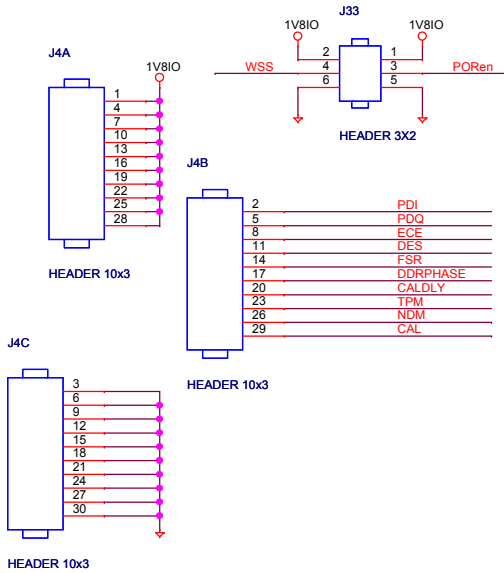
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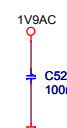
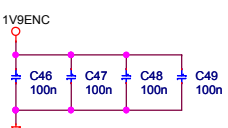
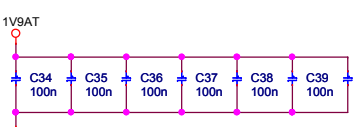
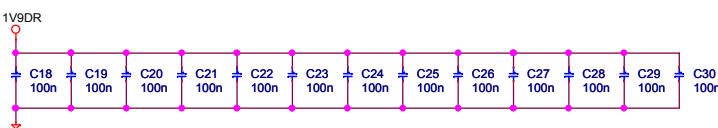
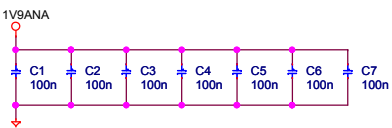
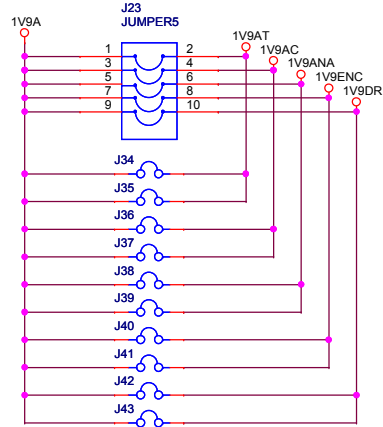
PRELIMINARY

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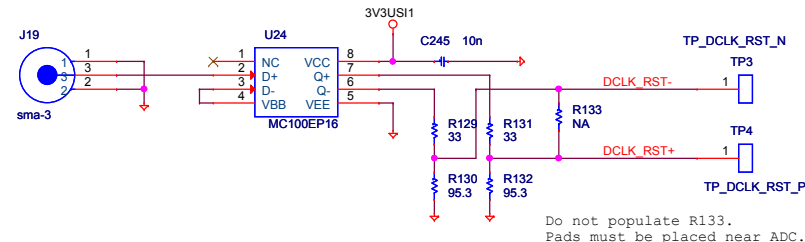




Power Supply Jumper



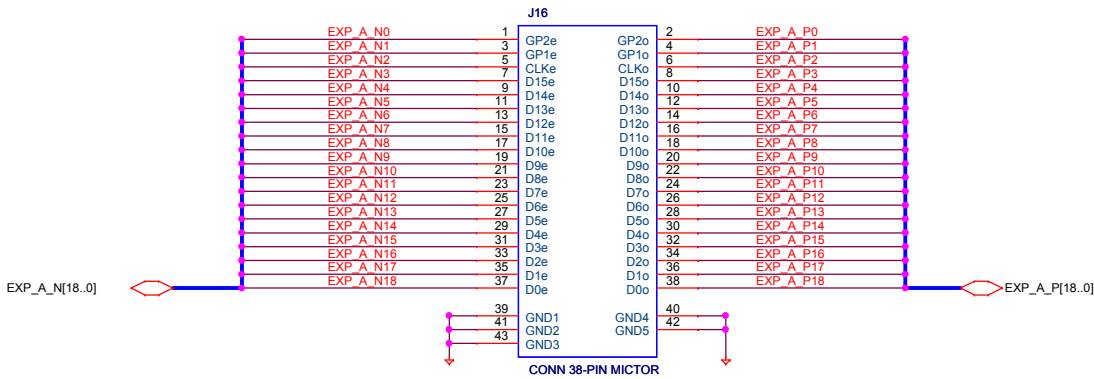
DCLK_RST SINGLE ENDED INPUT



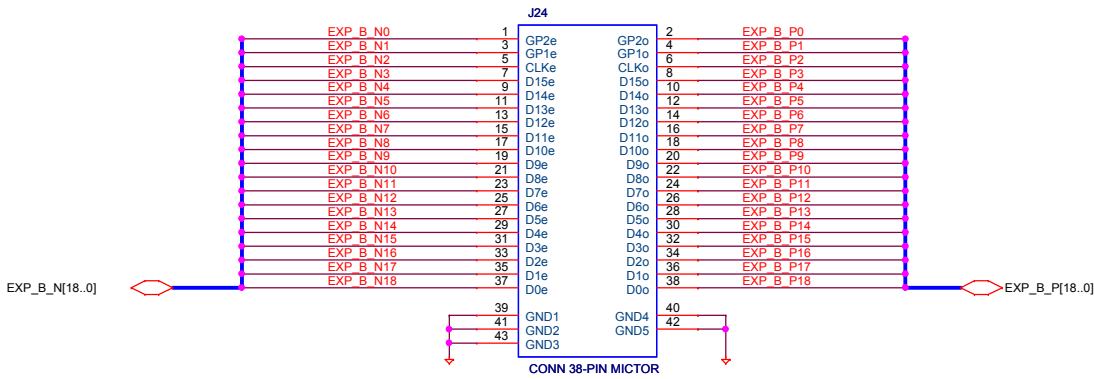
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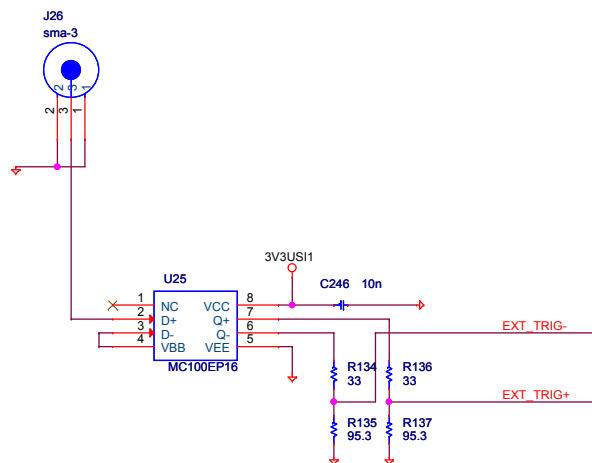
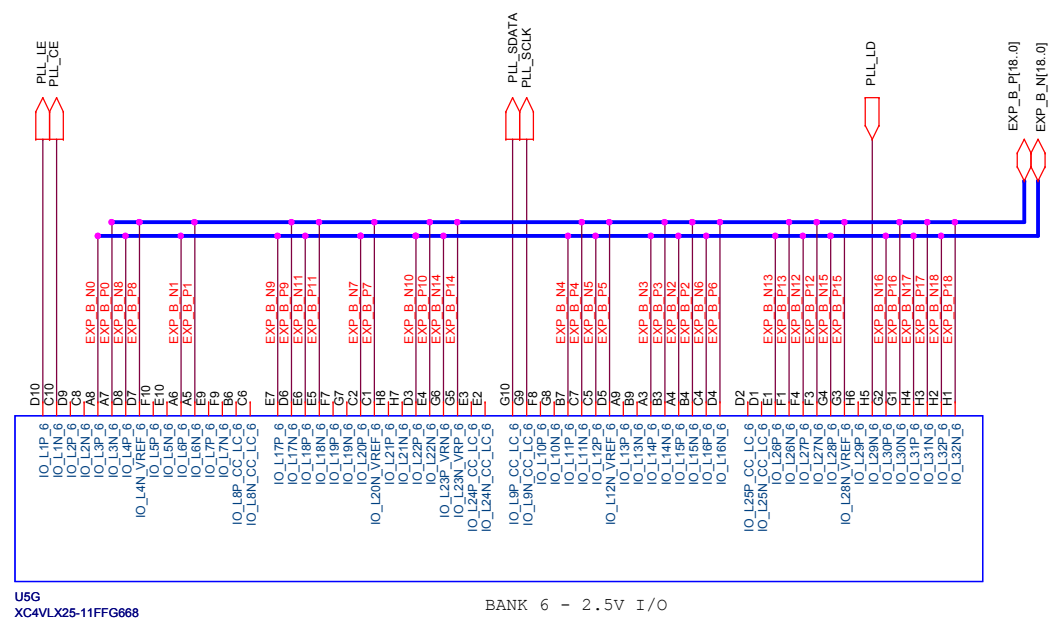
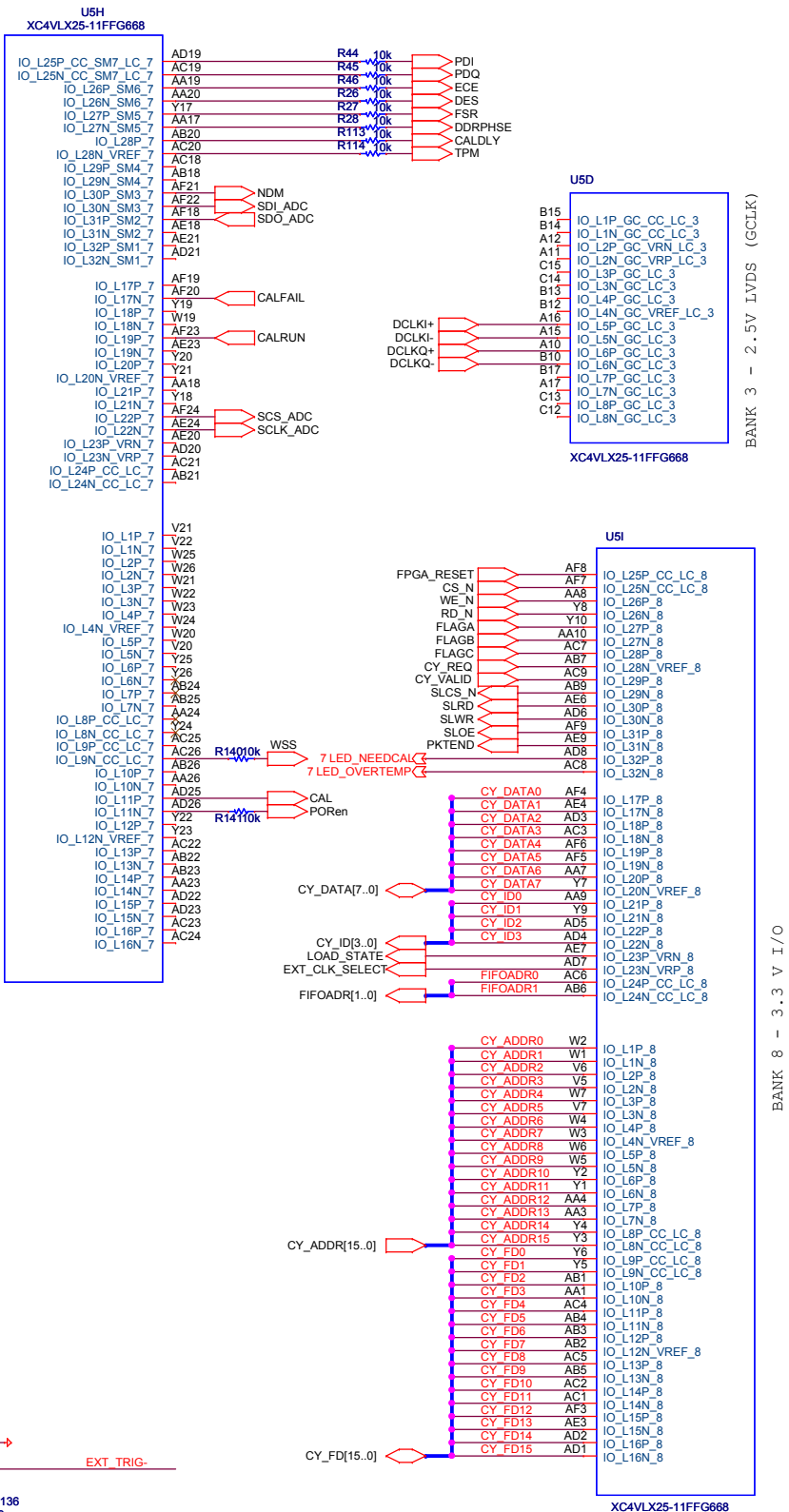
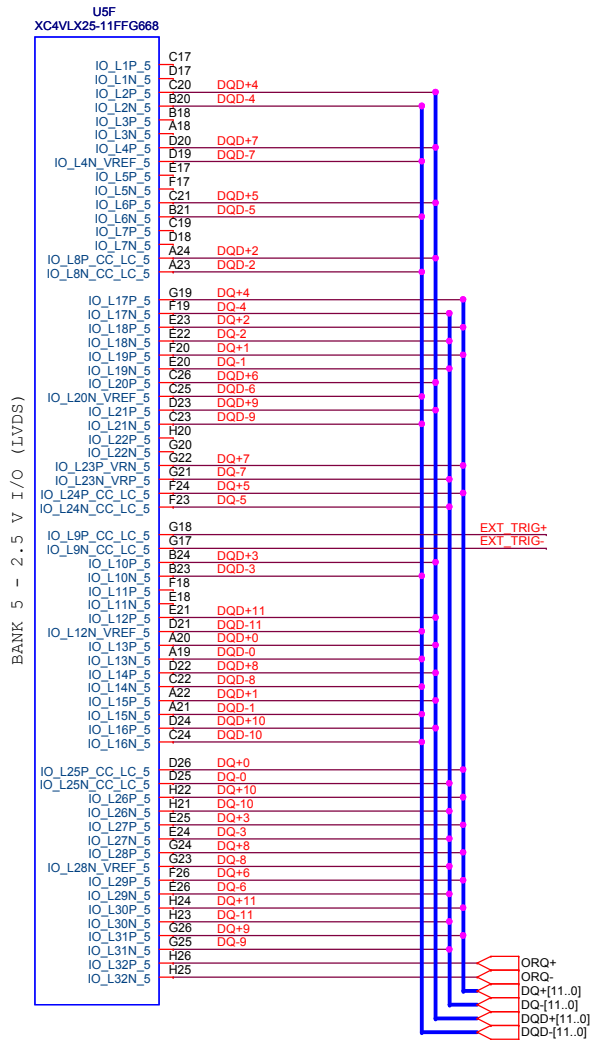
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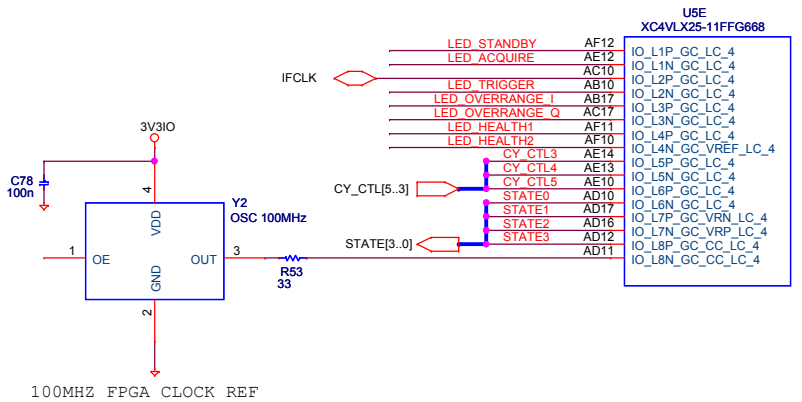
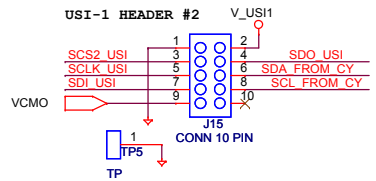
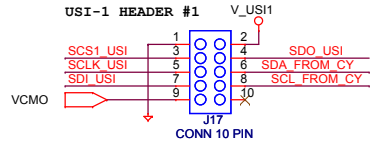
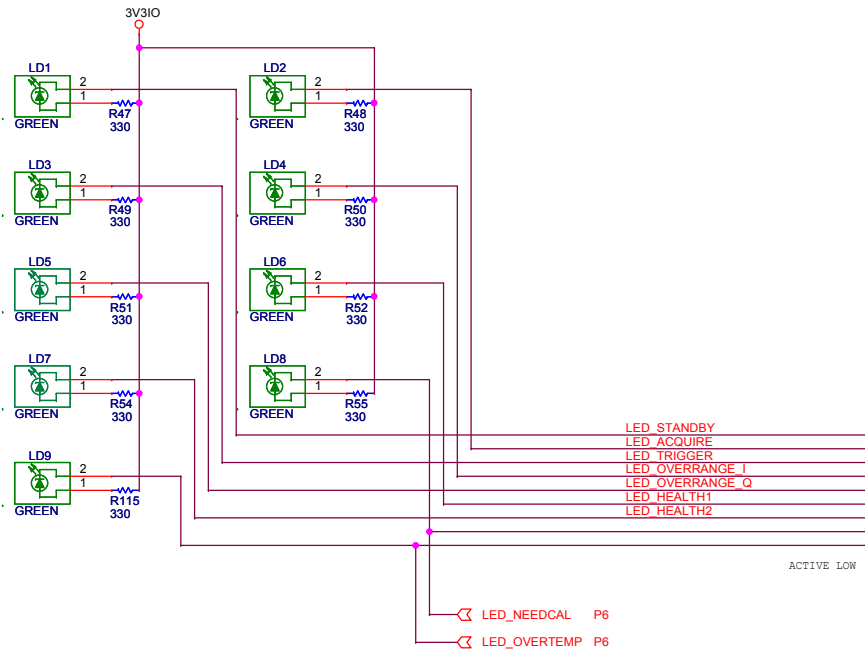
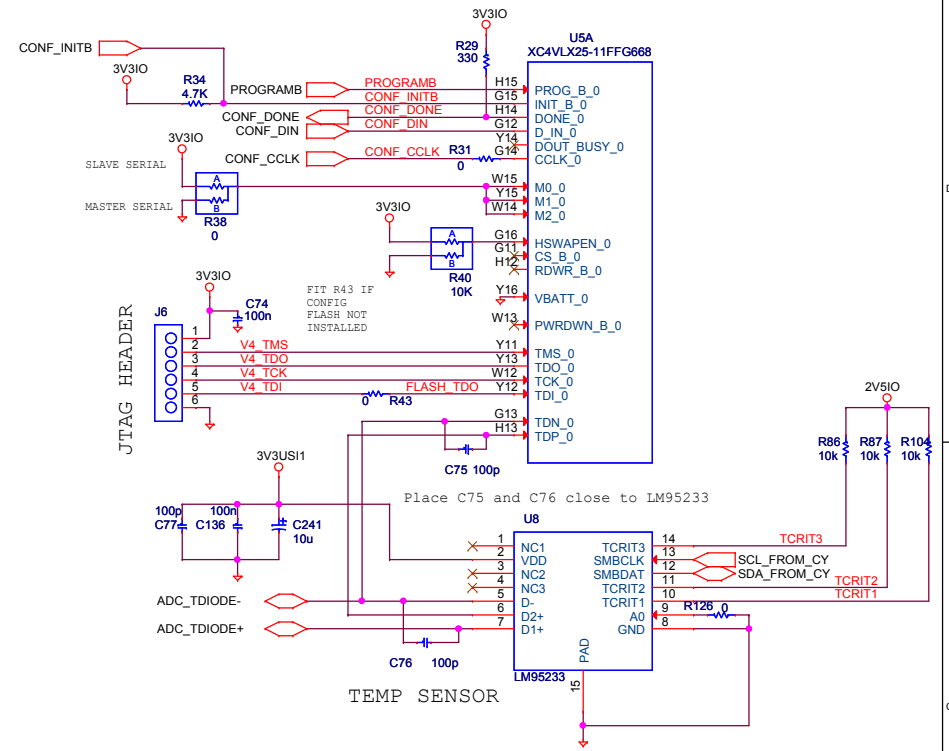
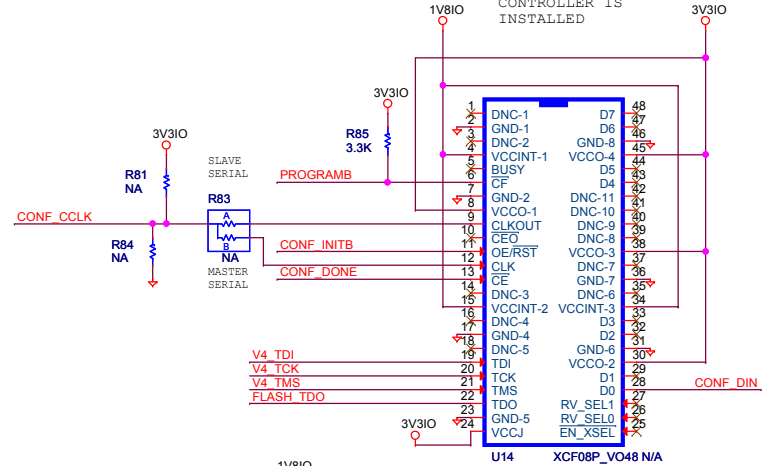
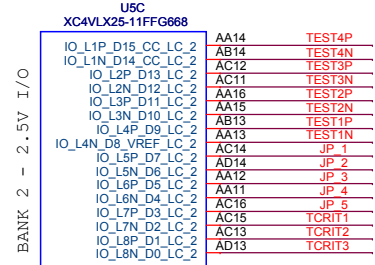
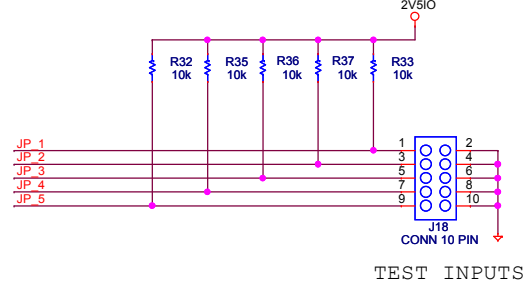
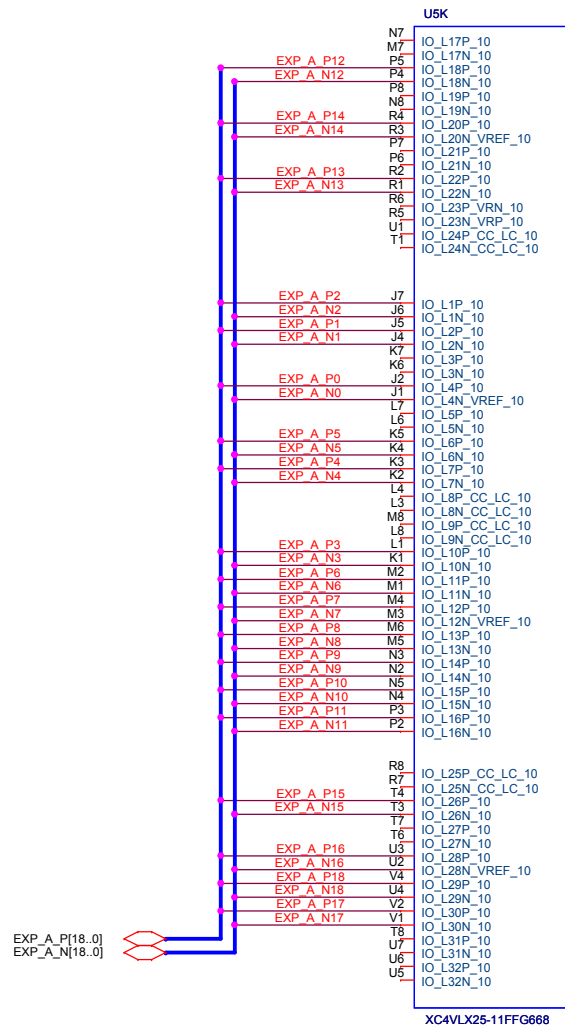
LOGIC ANALYZER HEADER



LOGIC ANALYZER HEADER







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The Sight & Sound of Information

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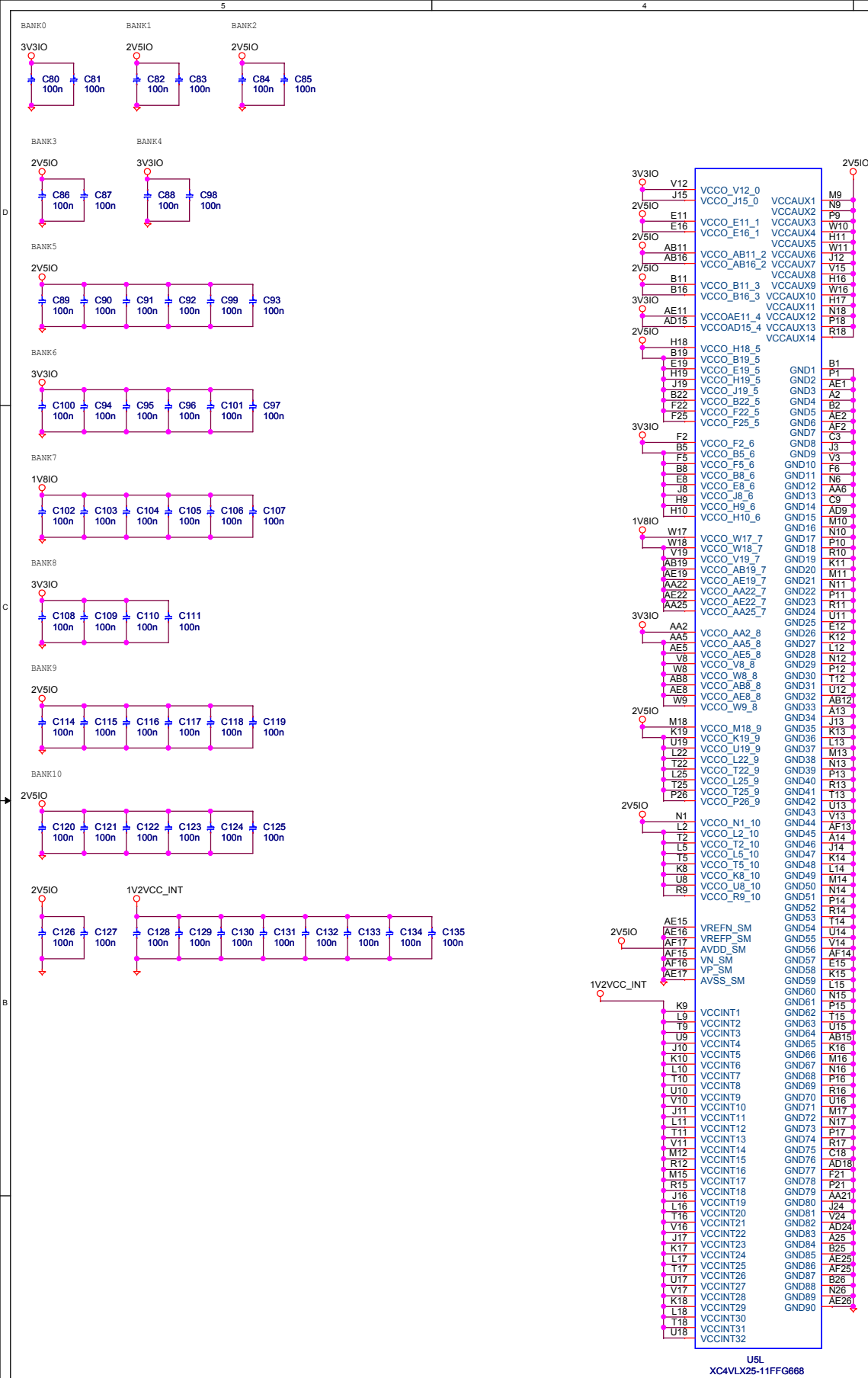
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FPGA2

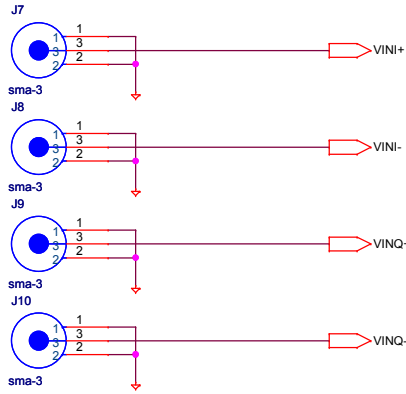
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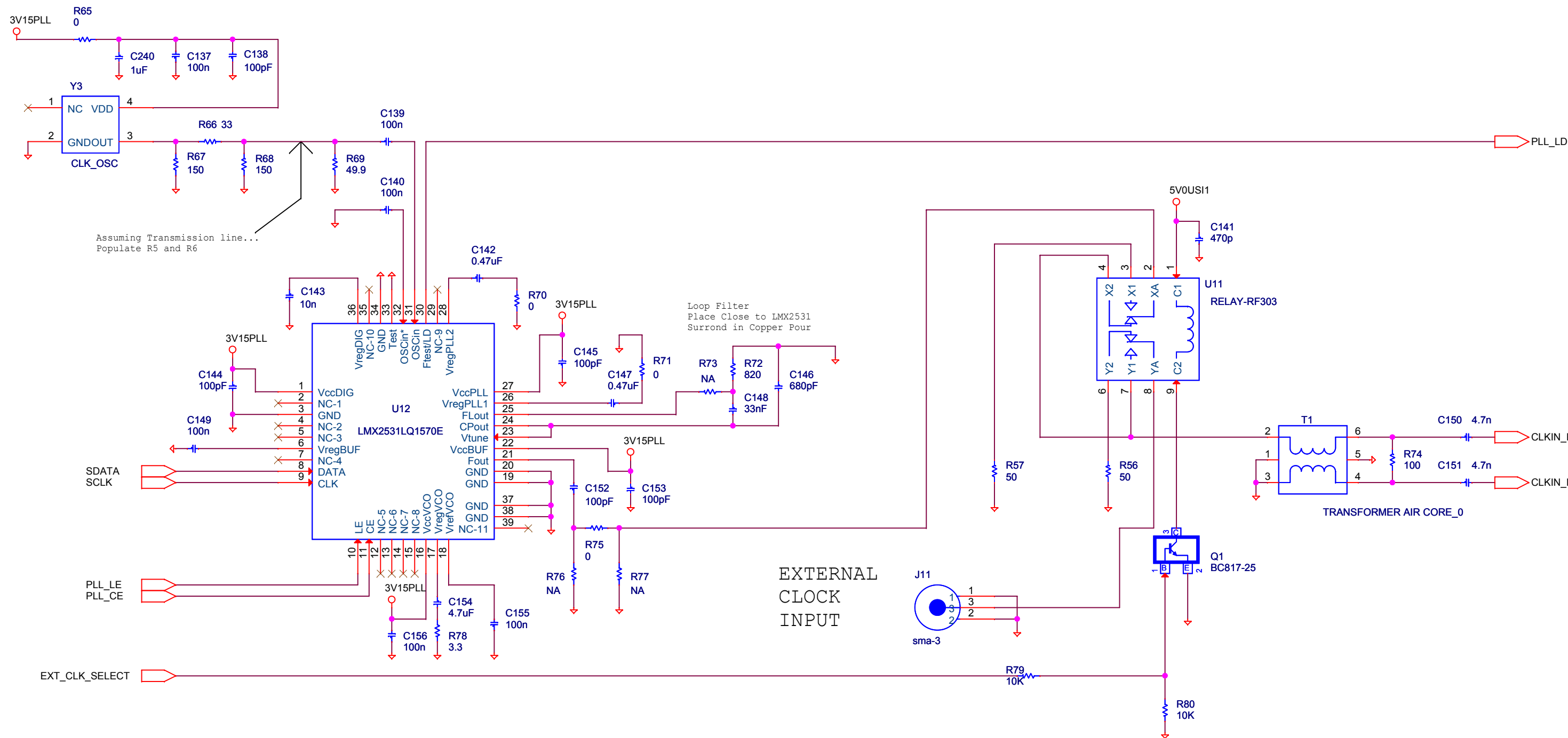
BANK #	BANK SUPPLY	INTERFACE
1	2V5IO	Clock Generator
2	2V5IO	Test Headers, Temp. Sensor
3	2V5IO	Cypress, LEDs, 100MHz Oscillator
4	3V3IO	ADC DCLK (LVDS)
5	2V5IO	ADC Q-Channel (LVDS)
6	3V3IO	USI-1 Header
7	1V8IO	ADC Control
8	3V3IO	Cypress, LEDs
9	2V5IO	ADC I-Channel (LVDS)
10	2V5IO	Logic Analyzer Header


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	PROJECT NAME: ADC12D800RFRB	PAGE TITLE FPGA3
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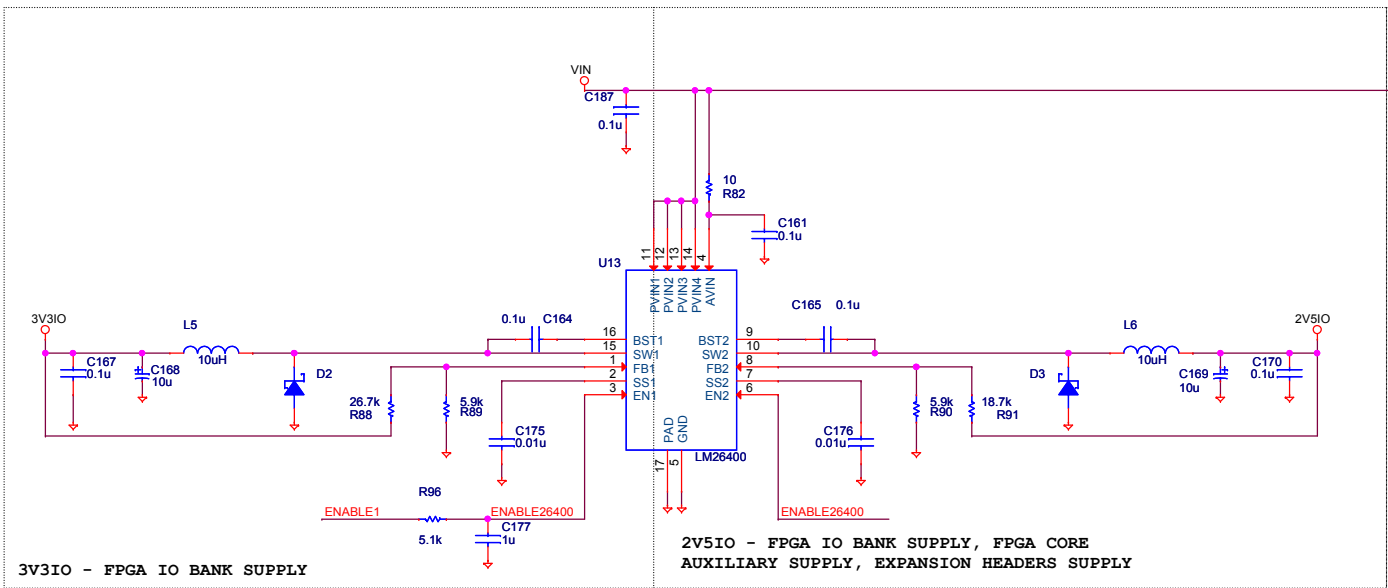


Impedance test connectors

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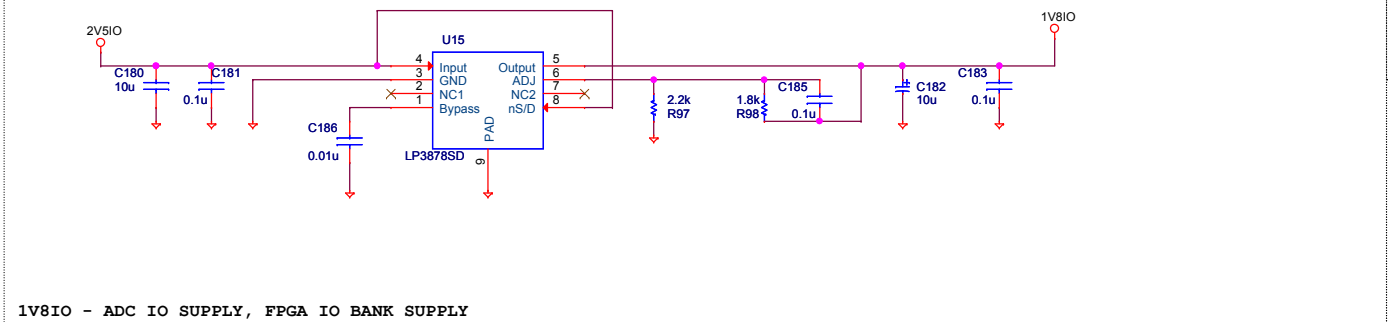


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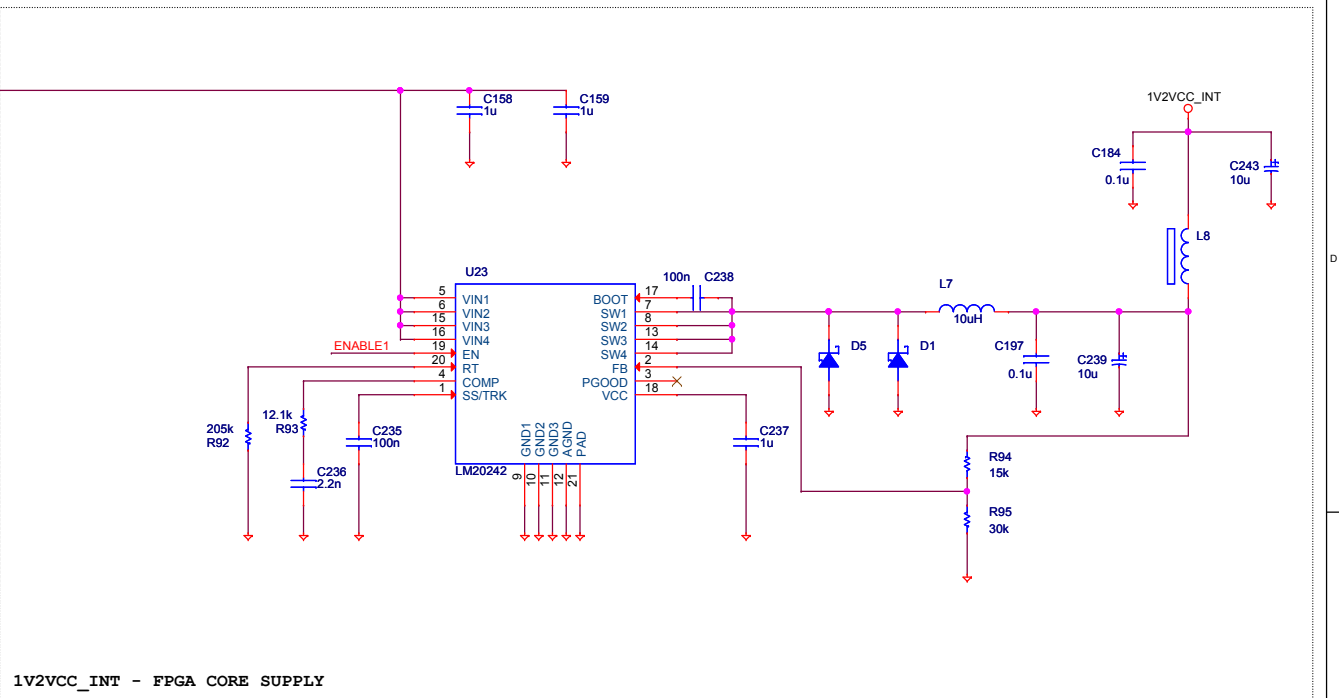


3V3IO - FPGA IO BANK SUPPLY

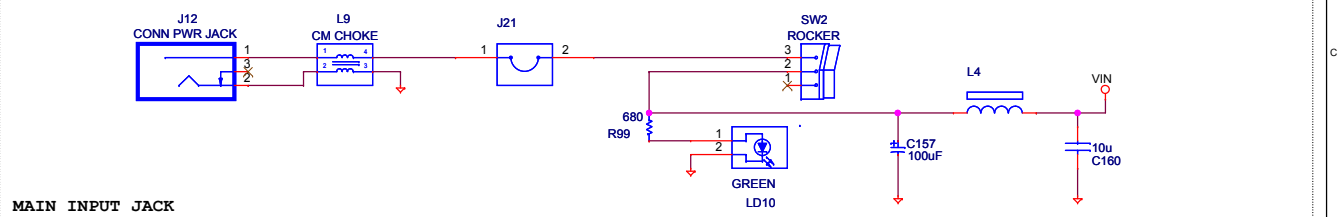
2V5IO - FPGA IO BANK SUPPLY, FPGA CORE
AUXILIARY SUPPLY, EXPANSION HEADERS SUPPLY



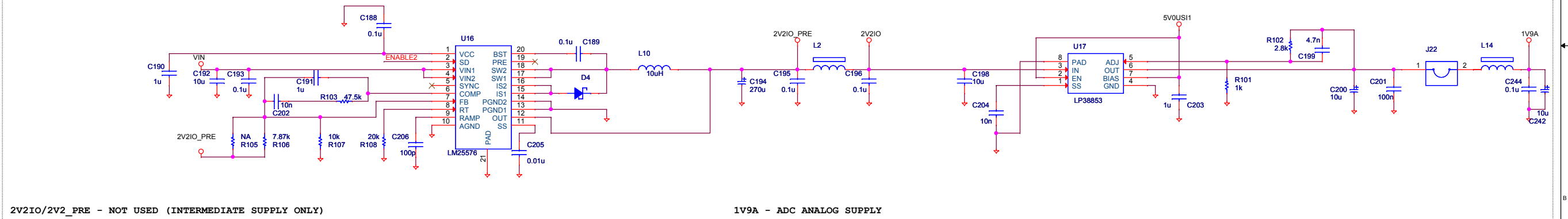
1V8IO - ADC IO SUPPLY, FPGA IO BANK SUPPLY



1V2VCC_INT - FPGA CORE SUPPLY

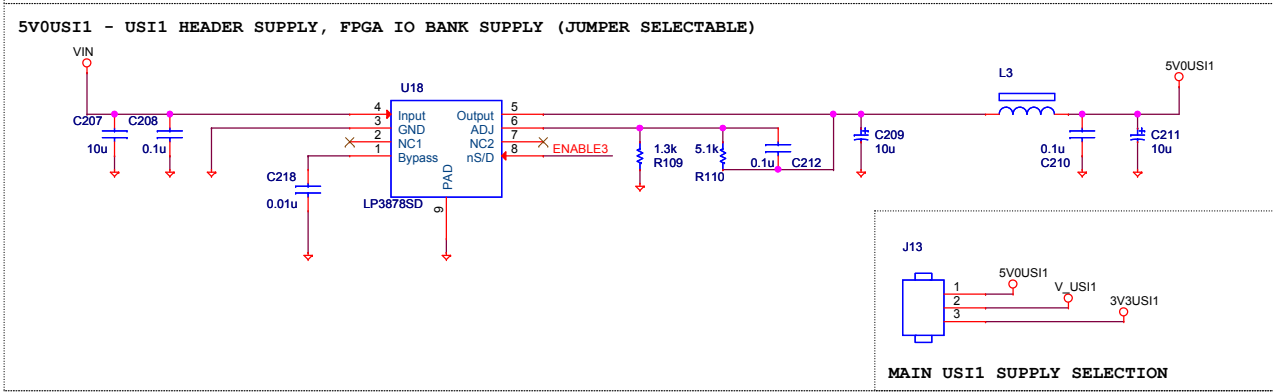


MAIN INPUT JACK



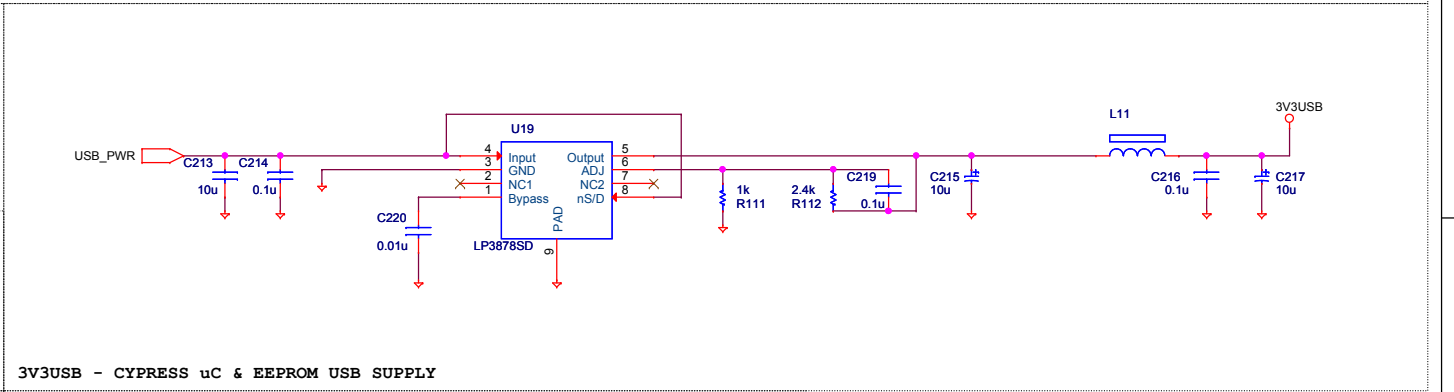
2V2IO/2V2_PRE - NOT USED (INTERMEDIATE SUPPLY ONLY)

1V9A - ADC ANALOG SUPPLY

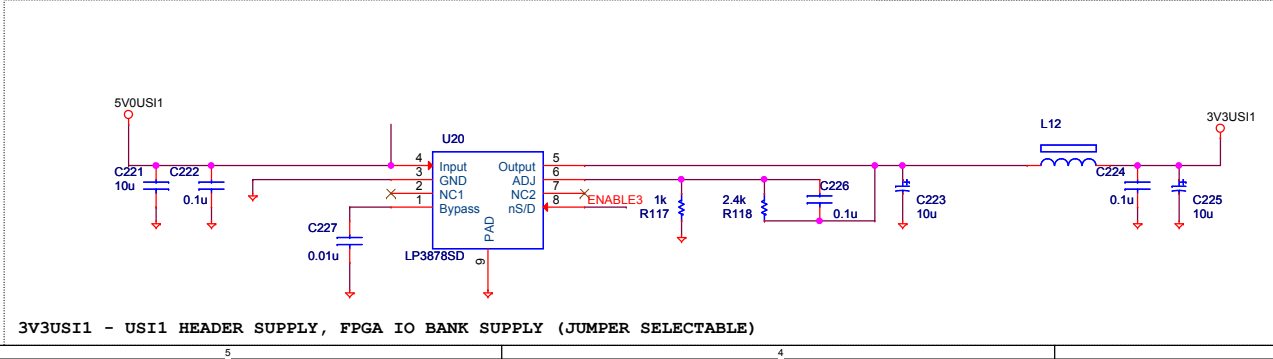


5V0USI1 - USI1 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)

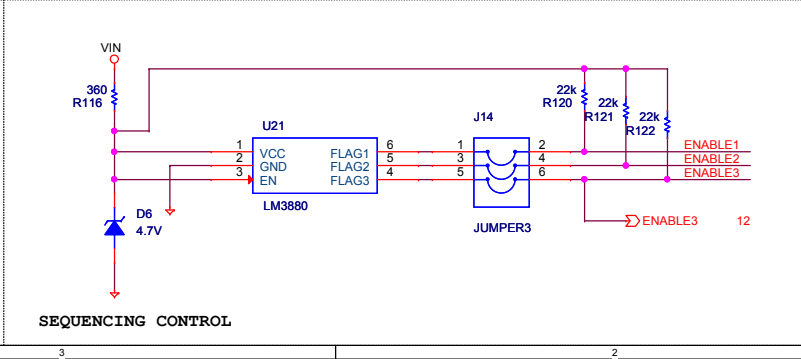
MAIN USI1 SUPPLY SELECTION



3V3USB - CYPRESS uC & EEPROM USB SUPPLY



3V3USI1 - USI1 HEADER SUPPLY, FPGA IO BANK SUPPLY (JUMPER SELECTABLE)



SEQUENCING CONTROL

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